

# MEMORY DEVICE CAPABLE OF CALIBRATION AND CALIBRATION METHODS THEREFOR

## 1 TECHNICAL FIELD

2 The technical field relates to memory devices capable of calibrating write currents  
3 in order to compensate for temperature variations.

## 4 BACKGROUND

5 Magnetic Random Access Memory (MRAM) is a proposed type of non-volatile  
6 memory. MRAM devices allow faster data access than conventional storage devices such  
7 as hard drives. Figure 1 illustrates a conventional MRAM memory array 10 having  
8 resistive memory cells 12 located at cross points of row conductors 14 and column  
9 conductors 16. Each memory cell 12 is capable of storing the binary states of "1" and  
10 "0."

11 Figure 2 illustrates a conventional MRAM memory cell 12. The memory cell 12  
12 includes a pinned layer 24 and a free layer 18. The pinned layer 24 has a magnetization  
13 of fixed orientation, illustrated by the arrow 26. The magnetization of the free layer 18,  
14 illustrated by the bi-directional arrow 28, can be oriented in either of two directions along  
15 an "easy axis" of the free layer 18. The magnetizations of the free layer 18 and the  
16 pinned layer 24 can be either "parallel" or "antiparallel" to one another. The two  
17 orientations correspond to the binary states of "1" and "0," respectively. The free layer  
18 18 and the pinned layer 24 are separated by an insulating tunnel barrier layer 20. The  
19 insulating tunnel barrier layer 20 allows quantum mechanical tunneling to occur between  
20 the free layer 18 and the pinned layer 24. The tunneling is electron spin dependent,  
21 making the resistance of the memory cell 12 a function of the relative orientations of the  
22 magnetizations of the free layer 18 and the pinned layer 24.

23 Each memory cell 12 in the memory array 10 can have its binary state changed by  
24 a write operation. Write currents  $I_x$  and  $I_y$  supplied to the row conductor 14 and the  
25 column conductor 16 crossing at a selected memory cell 12 switch the magnetization of  
26 the free layer 18 between parallel and antiparallel with the pinned layer 24. The current  
27  $I_y$  passing through the column conductor 16 results in the magnetic field  $H_x$ , and the  
28 current  $I_x$  passing through the row conductor 14 results in the magnetic field  $H_y$ . The  
29 fields  $H_x$  and  $H_y$  combine to switch the magnetic orientation of the memory cell 12 from  
30 parallel-to-antiparallel. A current  $-I_y$  is applied along with the current  $I_x$  to switch the  
31 memory cell 12 back to parallel.

1           In order to switch the state of the memory cell 12 from parallel-to-antiparallel, and  
2 vice versa, the combined field resulting from  $\pm H_x$  and  $H_y$  exceeds a critical switching  
3 field  $H_c$  of the memory cell 12. If  $H_x$  and  $H_y$  are too small, they will not switch the  
4 orientation of the selected memory cell 12. If either  $H_x$  or  $H_y$  is too large, memory cells  
5 12 on the row conductor 14 or the column conductor 16 of the selected memory cell 12  
6 may be switched by the action of either  $H_x$  or  $H_y$  acting alone. Memory cells 12  
7 subjected to either  $H_x$  or  $H_y$  alone are referred to as "half-selected" memory cells.

8           A problem may arise in MRAM arrays because the operational modes of an  
9 MRAM array and operating ambient temperature changes may cause the temperature of  
10 the MRAM array to vary, which would cause the coercivities of the memory cells to  
11 change. A change in coercivity of the memory cells changes the critical switching field  
12  $H_c$ , which in turn changes the fields  $H_x$  and  $H_y$  required to switch the state of the cells.  
13 Temperature-dependent changes in critical switching field  $H_c$  increase the likelihood that  
14 an entire row or column of half-selected memory cells will be programmed due to the  
15 action of  $I_x$  or  $I_y$  alone, or, the likelihood that the write currents  $I_x$  and  $I_y$  acting together  
16 will be insufficient to switch a selected memory cell.

## 17 SUMMARY

18           According to a first embodiment, a memory device comprises a substrate, an array  
19 of memory cells disposed over the substrate, a plurality of first conductors, a plurality of  
20 second conductors, wherein the first conductors cross the second conductors at the  
21 memory cells, a first current source selectively coupled to the first conductors and capable  
22 of providing a first write current to selected first conductors, a second current source  
23 selectively coupled to the second conductors and capable of providing a second write  
24 current to selected second conductors, a controller for controlling the application of the  
25 first and second write currents to the array of memory cells, and a temperature sensor  
26 disposed in the memory device. The temperature sensor senses a temperature of the  
27 memory device, and data from the temperature sensor are used to update the first and  
28 second write currents according to the sensed temperature.

29           According to a second embodiment, a method of calibrating a memory device  
30 comprises detecting a temperature of the memory device, determining whether the  
31 temperature of the memory device has changed by a threshold value, and updating at least  
32 one write current value if the temperature of the memory device changes by the threshold  
33 value.

1 According to a third embodiment, a method of filling a table with write current  
2 values for use in a memory device comprises applying a first write current and a second  
3 write current to conductors crossing at a reference memory cell when the memory array is  
4 at a temperature, detecting a state of the reference memory cell, increasing the first write  
5 current and the second write current if the state of the reference memory cell does not  
6 change, repeating the above steps until the state of the reference memory cell changes  
7 from a first state to a second state, and storing the first write current value and the second  
8 write current value that cause the state of the reference memory cell to change, wherein  
9 the first and second write current values are associated with the temperature.

10 Other aspects and advantages will become apparent from the following detailed  
11 description, taken in conjunction with the accompanying figures.

## 12 **DESCRIPTION OF THE DRAWINGS**

13 The detailed description will refer to the following drawings, in which like  
14 numerals refer to like elements, and in which:

15 Figure 1 illustrates a conventional memory array;

16 Figure 2 illustrates binary states of a conventional memory cell;

17 Figure 3 is a schematic view of an embodiment of a memory device;

18 Figure 4 is a plot of coercivity, or critical switching current, versus temperature  
19 for a memory cell;

20 Figure 5 is a flow chart illustrating a method of calibrating a memory device;

21 Figure 6 is a flow chart illustrating a method of updating write currents according  
22 to the method illustrated in Figure 5;

23 Figure 7 is a flow chart illustrating a method of filling a lookup table;

24 Figure 8 is a flow chart illustrating an alternative method of calibrating a memory  
25 device; and

26 Figure 9 is a flow chart illustrating a method of updating write currents according  
27 to the method illustrated in Figure 8.

## 28 **DETAILED DESCRIPTION**

29 A memory device capable of calibration to compensate for temperature variations  
30 and a calibration method will be discussed by way of preferred embodiments and by way  
31 of the figures.

32 Figure 3 is a schematic view of a cross point memory device 50 according to one  
33 embodiment. The memory device 50 includes a controller 52, a column decoder 54, a  
34 row decoder 56, a memory array 100, a bank 200 of write select switches, a bank 300 of

1 read/write select switches, a bank 400 of read/write select switches, a bank 500 of write  
2 termination select switches, a sense amplifier 600, and current sources 702, 704, 800.  
3 The memory device 50 also includes a temperature sensor 150 and a reference memory  
4 cell 160 used to calibrate the memory device 50.

5       The controller 52 controls read and write operations of the memory device 50.  
6 The controller 52 is coupled to the row decoder 56 to transmit commands to the row  
7 decoder 56, including read/write (R/W) data and row address data. The row decoder 56 is  
8 coupled to the gates of the switches in the switch banks 400 and 500, and opens and  
9 closes the switches in accordance with the controller 52 instructions. Similarly, the  
10 controller 52 is coupled to the column decoder 54, which is coupled to the gates of the  
11 switches in the switch banks 200, 300. The switches of the memory device 50 are  
12 illustrated as transistors. However, switches such as, for example, FET or MOSFET  
13 switches, and other switches, can also be used. The controller 52 can also be coupled to  
14 the temperature sensor 150 and the reference memory cell 160 to control calibration of  
15 the memory device 50.

16       The memory array 100 stores data for the memory device 50. In the memory  
17 array 100, row conductors 110 extend in horizontal rows, and column conductors 120  
18 extend in vertical columns. The row conductors 110 cross the column conductors 120 at  
19 memory cells 130. Each memory cell 130 can store the binary states 1 and 0. In Figure  
20 3, three rows of row conductors 110 and eight columns of column conductors 120,  
21 intersecting at twenty-four memory cells 130, are shown for the purposes of illustration.  
22 In practice, arrays of 1024 x 1024 or more memory cells may be used.

23       The bank 200 of write select switches selectively couples the column conductors  
24 120 to column write currents  $I_{yAP}$  or  $I_y$  from the current source 702, or to ground via a  
25 switch 214. A switch 212 selectively couples the column write current source 702 to the  
26 bank 200 of write select switches. The bank 300 of read/write select switches selectively  
27 couples the column conductors 120 to column write currents  $I_{yPA}$  or  $I_y$  from the current  
28 source 704, or to ground via a switch 314. The bank 300 also selectively couples the  
29 column conductors 120 to the sense amplifier 600. The bank 400 of read/write select  
30 switches selectively couples the row conductors 110 to a read voltage  $V_r$  through a switch  
31 414, and to row write currents  $I_{xAP}$ ,  $I_{xPA}$  or  $I_x$  via a switch 412. The bank 500 of write  
32 termination select switches selectively couples the row conductors 110 to ground. The  
33 current source 800 coupled to the bank 400 serves as a row write current source.

1           Writing to, or “programming” the memory cells 130 will now be discussed. In the  
2 discussion below, the subscript “PA” indicates programming a memory cell 130 from  
3 parallel-to-antiparallel, and the subscript “AP” indicates programming a memory cell 130  
4 from antiparallel-to-parallel. In order to write a state of 1, or an antiparallel state, to a  
5 memory cell 130 in the memory array 100, the column write current  $I_{yPA}$  is supplied to  
6 the column conductor 120 of the column in which the selected memory cell 130 is  
7 located, from the current source 702. The row write current  $I_{xPA}$  is simultaneously  
8 supplied to the row conductor 110 of the row in which the selected memory cell 130 is  
9 located. The banks 500 and 300 connect the respective currents conductors 110, 120 to  
10 ground. The magnetic fields  $H_y$  and  $H_x$  generated by the write currents  $I_{xPA}$  and  $I_{yPA}$   
11 combine to change the binary state of the memory cell 130 from 0 to 1. To write a bit of  
12 0 to a memory cell 130, the row write current  $I_{xAP}$  is applied as above, and the column  
13 write current  $I_{yAP}$  is applied from the current source 704. The bank 200 connects the  
14 current  $I_{yAP}$  to ground.

15           According to methods of programming discussed above, the column write  
16 currents  $I_{yAP}$  and  $I_{yPA}$  used to program a memory cell 130 can be of differing magnitude.  
17 The row write currents  $I_{xAP}$  and  $I_{xPA}$  can also have different magnitudes.

18           The memory device 50 can also operate using a single  $I_x$  value and a single  $I_y$   
19 value for parallel-to-antiparallel and antiparallel-to-parallel programming. In this case, to  
20 write a bit of 1 to a memory cell 130,  $I_y$  is applied from the current source 702, and  $I_x$  is  
21 applied from the current source 800. To write a bit of 0,  $I_y$  is applied from the current  
22 source 704, and  $I_x$  is applied from the current source 800.  $I_y$  supplied from the current  
23 source 704 may be referred to as “ $-I_y$ ”.

24           During operation of the memory device 50, read and write operations generate  
25 heat in the memory array 100. In addition, support circuitries in the memory device 50  
26 generate heat. These factors, along with the changing ambient temperature of the  
27 operating environment, and other factors, may cause the temperature of the memory  
28 device 50 to vary. The changing temperature causes the coercivities, and therefore the  
29 critical switching fields  $H_c$  of the memory cells 130, to vary during operation of the  
30 device 50.

31           In order to compensate for changes in memory cell critical switching field  $H_c$ , the  
32 memory device 50 includes the temperature sensor 150 and the reference memory cell  
33 160. The controller 52 may be coupled to the temperature sensor 150 to accept  
34 temperature data from the temperature sensor 150. The controller 52 can use data from

1 the temperature sensor 150 and the reference memory cell 160 to calibrate the write  
2 currents  $I_{YAP}$ ,  $I_{YPA}$ ,  $I_{XAP}$  and  $I_{XPA}$ , or  $I_x$  and  $I_y$  as the temperature of the array 100 varies.  
3 The temperature sensor 150 can be located anywhere in the memory device 50 where the  
4 temperature of the memory cells 130 can be detected. In one embodiment, the  
5 temperature sensor 150 is located beneath the memory array 100. For example, the  
6 memory device 50 can comprise a semiconductor substrate (not illustrated), and the  
7 temperature sensor 150 can be disposed over the substrate in the vicinity of the memory  
8 cells 130, or in other locations. The temperature of the array 100 may be relatively  
9 uniform across the array 100, and it may therefore not be necessary to place the  
10 temperature sensor 150 in close proximity to the memory cells 130. Multiple temperature  
11 sensors 150 can also be used, with sensors 150 located in multiple locations in the  
12 memory device 50. If multiple temperature sensors 150 are used, the controller 52 can,  
13 for example, utilize an average of temperature readings from the sensors 150.

14 The reference memory cell 160 can also be at any location in the memory device  
15 50. The reference memory cell 160 may be located at the cross point of a first conductor  
16 161 and a second conductor 162. The first conductor 161 can be coupled to the banks  
17 200 and 300 of switches, and the second conductor 162 can be coupled to the banks 400  
18 and 500 of switches. By these connections, the state of the reference memory cell 160  
19 can be changed by the action of  $I_{YAP}$ ,  $I_{YPA}$ ,  $I_{XAP}$  and  $I_{XPA}$ , or  $I_x$  and  $I_y$  in the same manner  
20 that the memory cells 130 are programmed. The reference memory cell 160 can also be  
21 connected to a read voltage  $V_r$  through the bank 400 of read/write select switches, and to  
22 the sense amplifier 600 through the bank 300 of read/write select switches. The  
23 controller 52 can therefore detect the state of the reference memory cell 160 from the  
24 output of the sense amplifier 600.

25 Operation of the reference memory cell 160 and the temperature sensor 150 is  
26 discussed in further detail below. Figure 4 illustrates coercivity characteristics of the  
27 memory cells 130 that render calibration using the memory cell 160 and the temperature  
28 sensor 150 advantageous.

29 Figure 4 is a plot of coercivity ( $O_e$ ), or critical switching field  $H_c$ , versus  
30 temperature for a memory cell 130. The critical switching field  $H_c$  for switching a  
31 memory cell 130 from antiparallel-to-parallel decreases with increasing temperature. The  
32 critical switching field  $H_c$  for switching a memory cell 130 from parallel-to-antiparallel  
33 increases with increasing temperature. In both cases, the magnitude of  $H_c$  decreases with  
34 increasing temperature. During operations of the memory device 50, such as when the

1 device is in, for example, a standby mode or a read mode, the temperature of the memory  
2 array 100 may be different from when the memory device is in a write mode. The  
3 temperature of the memory array 100 may also vary while the array is in any of the above  
4 modes. The temperature variations in the memory array 100 therefore change the  
5 required magnitudes of the write currents  $I_{yPA}$  and  $I_{xPA}$ , or  $I_{yAP}$  and  $I_{xAP}$ . The switching  
6 data in Figure 4 illustrate that the coercivity curves for switching a memory cell 130 from  
7 antiparallel-to-parallel and vice versa can be nonlinear. In addition, the antiparallel-to-  
8 parallel switching curve may also be asymmetric about the zero coercivity axis with  
9 respect to the parallel-to-antiparallel switching curve. If the switching curves are  
10 asymmetric,  $I_{yPA}$  and  $I_{xPA}$  for parallel-to-antiparallel switching at temperature  $T$  will differ  
11 in magnitude from  $I_{yAP}$  and  $I_{xAP}$  for antiparallel-to-parallel switching at the same  
12 temperature  $T$ .

13 Figure 5 is a flow chart illustrating a method of calibrating a memory device to  
14 compensate for temperature variations in the memory device. The method can be used,  
15 for example, to calibrate the memory device 50 illustrated in Figure 3, or to calibrate  
16 other cross point memory devices. The calibration method can be used to calibrate the  
17 write currents  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$ , and can be executed by the controller 52 of the  
18 memory device 50.

19 In step S10, a temperature  $T$  of the memory array 100 is detected by the  
20 temperature sensor 150. Temperature detection can be performed, for example,  
21 periodically.

22 In step S12, the temperature  $T$  of the memory array 100 is compared with a  
23 calibration temperature  $T_c$  to determine whether the difference between the temperature  $T$   
24 of the memory array 100 and the calibration temperature  $T_c$  is greater than a threshold  
25 temperature change value  $\Delta T$ . Step S12 is executed to determine whether the temperature  
26  $T$  of the memory array 100 has risen or fallen a sufficient amount to change the  
27 coercivities of the memory cells 130 sufficiently to require an update of the write currents  
28  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  used to write to the memory cells 130. The calibration temperature  
29  $T_c$  can be set as an initial reference value when the memory device 50 is activated. When  
30 the memory device 50 is activated, the write currents  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  may be selected  
31 to be appropriate to write to the memory cells 130 at the initial calibration temperature  $T_c$ .  
32 A suitable initial value for  $T_c$  can be, for example, room temperature.

33 If  $|T - T_c|$  does not exceed the threshold temperature change value  $\Delta T$ , the  
34 method returns to step S10. The threshold temperature change value  $\Delta T$  can be selected,

1 for example, so that relatively small changes in the temperature  $T$  of the memory array  
2 100 do not result in updating of the write currents  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$ . Step S10 can be  
3 performed, for example, periodically, according to any desired degree of accuracy for the  
4 calibration process.

5 If  $|T - T_c|$  exceeds the threshold temperature change value  $\Delta T$ , the method  
6 proceeds to step S14. In step S14, the write currents  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  are updated to  
7 compensate for coercivity changes in the memory cells 130 caused by the change in  
8 temperature  $T$  of the memory array 100. The write currents  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  can be  
9 updated according to the method illustrated in Figure 6, in which data from the reference  
10 memory cell 160 are used to determine the appropriate  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values for the  
11 detected temperature  $T$ . The method illustrated in Figure 6 is discussed in detail below.  
12 Alternatively, the appropriate  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values associated with the detected  
13 temperature  $T$  can be selected from a lookup table. The lookup table can include, for  
14 example,  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values for each of the temperature  $T$  values that the  
15 memory array 100 may be expected to have during operation. A method of filling a  
16 lookup table with  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values associated with particular calibration  
17 temperature values  $T_c$  is discussed in detail below with reference to Figure 7.

18 After the  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values are updated in step S14, the calibration  
19 temperature  $T_c$  is updated in step S16. The calibration temperature  $T_c$  can be assigned  
20 the value of the present temperature  $T$  of the memory array 100 detected in step S10. The  
21 method then returns to step S10, where the temperature of the memory array 100 may be  
22 periodically monitored. Alternatively, the method can STOP when operation of the  
23 memory device 50 ceases.

24 According to the above method, at any time during operation of the memory  
25 device 50, appropriate  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values are available to write to a selected  
26 memory cell 130.

27 Figure 6 is a flow chart illustrating a method of updating write currents according  
28 to a first embodiment. The steps illustrated in Figure 6 comprise step S14 from Figure 5.  
29 The method illustrated in Figure 6 utilizes data from the reference memory cell 160 to  
30 determine appropriate  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values for the memory array 100 operating at a  
31 detected temperature  $T$ .

32 The method of updating write currents illustrated in Figure 6 assumes that the  
33 antiparallel-to-parallel switching (coercivity) curve may be asymmetric about the zero  
34 coercivity axis with respect to the parallel-to-antiparallel switching curve. If the



1 switching curves are asymmetric, appropriate  $I_{xPA}$  and  $I_{yPA}$  (currents used for parallel-to-  
2 antiparallel switching) for a temperature  $T$  will differ from  $I_{xAP}$  and  $I_{yAP}$  (currents used for  
3 antiparallel-to-parallel switching) for the same temperature  $T$ .

4 The method begins with a determination of  $I_{xPA}$  and  $I_{yPA}$ . In step S30, arbitrarily  
5 low initial currents of  $I_{xPA}$  and  $I_{yPA}$  are applied at the first and second conductors 161, 162  
6 crossing at the reference memory cell 160. The initial currents  $I_{xPA}$  and  $I_{yPA}$  should be  
7 small enough such that the reference memory cell 160 would not be expected to switch  
8 from parallel-to-antiparallel due to application of  $I_{xPA}$  and  $I_{yPA}$ . In step S32, the state of  
9 the reference memory cell 160 is detected. The state of the reference memory cell 160  
10 can be detected by applying a read voltage  $V_r$  to the second conductor 162 and  
11 connecting the first conductor 161 to the sense amplifier 600. The output of the sense  
12 amplifier 600 can be used to determine the state of the reference memory cell 160.

13 In step S34, it is determined whether the currents  $I_{xPA}$  and  $I_{yPA}$  caused the  
14 reference memory cell 160 to switch from a parallel to an antiparallel state. If the state of  
15 the reference memory cell 160 has not changed,  $I_{xPA}$  and  $I_{yPA}$  are increased by an  
16 incremental amount in step S36. The amount by which  $I_{xPA}$  and  $I_{yPA}$  are increased can be  
17 determined according to the degree of accuracy desired for the calibration process. The  
18 method then returns to step S30, where the increased currents  $I_{xPA}$  and  $I_{yPA}$  are applied to  
19 the reference memory cell 160. The process of incrementally increasing  $I_{xPA}$  and  $I_{yPA}$  is  
20 repeated until the state of the reference memory cell 160 changes. Then, at step S34,  
21 when a state change is detected, the method proceeds to step S38. In step S38,  $I_{xPA}$  and  
22  $I_{yPA}$  are updated to correspond to the values of  $I_{xPA}$  and  $I_{yPA}$  that caused the state of the  
23 reference memory cell 160 to change.

24 After  $I_{xPA}$  and  $I_{yPA}$  have been updated, the reference memory cell 160 is in the  
25 antiparallel state. The values  $I_{xAP}$  and  $I_{yAP}$  can then be determined.

26 In step S40, initial values of  $I_{xAP}$  and  $I_{yAP}$  are applied at the reference memory cell  
27 160. The state of the reference memory cell 160 is detected in step S42, and if the state is  
28 determined to be unchanged in step S44, the values  $I_{xAP}$  and  $I_{yAP}$  are increased by an  
29 incremental amount in step S46.  $I_{xAP}$  and  $I_{yAP}$  are increased iteratively until the state of  
30 the reference memory cell 160 changes under application of  $I_{xAP}$  and  $I_{yAP}$ . When the state  
31 of the reference memory cell 160 changes, the values  $I_{xAP}$  and  $I_{yAP}$  that caused the state  
32 change are set as the updated  $I_{xAP}$  and  $I_{yAP}$  values in step S48.

33 After the  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values have been updated in step S14, the updated  
34 values can be stored and used by the current sources 702, 704, 800. An optional

1 additional step may include increasing one or more of  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$  and  $I_{yAP}$  by a  
2 predetermined amount after updating in step S14. The predetermined amount can be  
3 added to  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$  and  $I_{yAP}$ , for example, to ensure switching of memory cells 130  
4 by the updated current values.

5 Figure 7 is a flow chart illustrating a method of filling a lookup table according to  
6 one embodiment. The lookup table values of  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  can be stored, and  
7 accessed in step S14 of the method illustrated in Figure 5.

8 In step S50, a calibration temperature variable  $T_c$  is set at an initial value  $T_{c0}$ . The  
9 initial temperature value  $T_{c0}$  can, for example, be at the lower end of an expected  
10 operating temperature range for the memory array 100. In step S52, the reference  
11 memory cell 160 is placed at the temperature  $T_c$ . The reference memory cell 160 can be  
12 placed at the calibration temperature  $T_c$  by appropriate heating or cooling of the memory  
13 array 100.

14 In step S54, values  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  for the present calibration temperature  $T_c$   
15 are determined using the reference memory cell 160. The values can be determined, for  
16 example, using steps S30 through S48, as illustrated in Figure 6.

17 In step S56, the current values  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  are stored. The values can be  
18 stored in any media accessible by the controller 52, including a media comprising a part  
19 of the controller 52, so that the current sources 702, 704, 800 can be instructed to generate  
20 the currents. The values for  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  are associated with the present  
21 calibration temperature  $T_c$ .

22 In step S58, the calibration temperature  $T_c$  is increased by an incremental amount  
23  $\delta T$ . The amount  $\delta T$  can be as small as necessary to obtain a desired degree of precision  
24 for the calibration process. The method then returns to step S52, where the temperature  
25 of the memory array 100 is raised to the new calibration temperature  $T_c$ , and values for  
26  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  are determined for the new calibration temperature  $T_c$  in step S54.

27 The process of determining  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  for each value  $T_c$  is repeated until  
28  $T_c$  reaches a value corresponding to an upper end of the expected operating temperature  
29 range for the memory array 100.

30 After  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  values have been generated for each calibration  
31 temperature value  $T_c$ , a complete lookup table of write current values for the memory  
32 array 100 has been generated. The lookup table, for example, is accessible in step S14 of  
33 the method illustrated in Figure 5.

1           As an alternative to starting the calibration process at a lower end of an expected  
2 operating temperature range of the memory device 50,  $T_{c0}$  may instead be set at an upper  
3 end of the expected operating temperature range. In this case,  $T_c$  is decreased by  $\delta T$  in  
4 step S58.

5           According to the methods illustrated in Figures 5-7, the memory device 50 can  
6 reliably switch the memory cells 130 of the memory array 100. Updating the write  
7 currents  $I_{xPA}$ ,  $I_{yPA}$ ,  $I_{xAP}$ ,  $I_{yAP}$  when temperature variations occur ensures that the  
8 appropriate switching fields  $H_x$  and  $H_y$  are applied when the temperature of the memory  
9 array 100 varies. In addition, by calculating separate values for parallel-to-antiparallel  
10 and antiparallel-to-parallel switching currents, the calibration method compensates for  
11 asymmetry in the switching curves for the memory cells 130.

12           The methods discussed above address the situation where the antiparallel-to-  
13 parallel switching curve for a memory cell 130 may be asymmetric about the zero  
14 coercivity axis with respect to the parallel-to-antiparallel switching curve (see discussion  
15 of Figure 4 above). Figure 8 is a flow chart illustrating an alternative method of  
16 calibrating a memory device, in which a memory array 100 may include memory cells  
17 having antiparallel-to-parallel switching curves that are substantially symmetric about a  
18 zero coercivity axis with respect to the parallel-to-antiparallel switching curve. Figure 9  
19 is a flow chart illustrating a method of updating write currents according to the method  
20 illustrated in Figure 8.

21           In step S70, a temperature  $T$  of the memory array 100 is detected by the  
22 temperature sensor 150. Temperature detection can be performed, for example,  
23 periodically.

24           In step S72, the temperature  $T$  of the memory array 100 is compared with a  
25 calibration temperature  $T_c$  to determine whether the difference between the temperature  $T$   
26 of the memory array 100 and the calibration temperature  $T_c$  is greater than a threshold  
27 temperature change value  $\Delta T$ . If  $|T - T_c|$  does not exceed the threshold temperature  
28 change value  $\Delta T$ , the method returns to step S70. If  $|T - T_c|$  exceeds the threshold  
29 temperature change value  $\Delta T$ , the method proceeds to step S74.

30           In step S74, the write currents  $I_x$  and  $I_y$  are updated to compensate for coercivity  
31 changes in the memory cells 130 caused by the change in temperature  $T$  of the memory  
32 array 100. The write currents  $I_x$  and  $I_y$  can be updated, for example, according to the  
33 method illustrated in Figure 9, in which data from the reference memory cell 160 is used  
34 to determine appropriate  $I_x$  and  $I_y$  values. The method illustrated in Figure 9 is discussed

1 in detail below. Alternatively, the appropriate  $I_x$  and  $I_y$  values for the detected  
2 temperature  $T$  can be selected from a lookup table.

3 After the  $I_x$  and  $I_y$  values are updated in step S74, the calibration temperature  $T_c$   
4 is updated in step S76. The calibration temperature  $T_c$  can be assigned the value of the  
5 present temperature  $T$  of the memory array 100 detected in step S70. The method then  
6 returns to step S70, where the temperature of the memory array 100 may be periodically  
7 monitored. Alternatively, the method can STOP when operation of the memory device  
8 ceases.

9 Figure 9 is a flow chart illustrating a method of updating write currents according  
10 to the method illustrated in Figure 8. The steps illustrated in Figure 9 comprise step S74  
11 from Figure 8. The method illustrated in Figure 9 utilizes data from the reference  
12 memory cell 160 to determine appropriate  $I_x$  and  $I_y$  values for the memory array 100  
13 operating at a detected temperature  $T$ . The method illustrated in Figure 9 assumes that the  
14 reference memory cell 160 is in a parallel state when calibration begins. If the reference  
15 memory cell 160 is initially in an antiparallel state,  $-I_y$ , instead of  $I_y$ , would be applied to  
16 change the state of the reference memory cell 160.

17 In step S80, arbitrarily low initial currents of  $I_x$  and  $I_y$  are applied at the first and  
18 second conductors 161, 162 crossing at the reference memory cell 160. In step S82, the  
19 state of the reference memory cell 160 is detected. The output of the sense amplifier 600  
20 can be used to determine the state of the reference memory cell 160.

21 In step S84, it is determined whether the currents  $I_x$  and  $I_y$  caused the reference  
22 memory cell 160 to switch from a parallel to an antiparallel state. If the state of the  
23 reference memory cell 160 has not changed,  $I_x$  and  $I_y$  are increased by an incremental  
24 amount in step S86. The method then returns to step S80, where the increased currents  
25  $I_x$  and  $I_y$  are applied to the reference memory cell 160. The process of incrementally  
26 increasing  $I_x$  and  $I_y$  is repeated until the state of the reference memory cell 160 is changed  
27 under application of  $I_x$  and  $I_y$  in step S80. Then, at step S84, when a state change is  
28 detected, the method proceeds to step S88. In step S88,  $I_x$  and  $I_y$  are updated to  
29 correspond to the values of  $I_x$  and  $I_y$  that caused the state of the reference memory cell  
30 160 to change.

31 As an alternative to calculating updated write currents  $I_x$  and  $I_y$  during the method  
32 illustrated in Figure 8,  $I_x$  and  $I_y$  values can be taken from a lookup table. The  $I_x$  and  $I_y$   
33 values can be calculated in a manner similar to the method illustrated in Figure 7.  
34 However, it is not necessary to calculate parallel-to-antiparallel and antiparallel-to-

1 parallel switching currents. In other words, a single state change, either from parallel-to-  
2 antiparallel, or from antiparallel-to-parallel, for each certain temperature  $T$ , can be used to  
3 fill the lookup table. The lookup table values of  $I_x$  and  $I_y$  can be stored, and accessed in  
4 step S74 of the method illustrated in Figure 8.

5 The calibration methods discussed above can be performed by the controller 52,  
6 or by any computing device capable of executing instructions. For example, an external  
7 processing device could be coupled to the memory device 52 to perform the calibration  
8 methods discussed above.

9 In the calibration methods discussed above, calibration is performed using a  
10 reference memory cell 160. The reference memory cell 160 can be a memory cell  
11 separate from the array 100 of memory cells 130 that are used to store data in the memory  
12 device 50. Alternatively, a memory cell 130 in the memory array 100 can function as the  
13 reference memory cell in the methods discussed above. If a memory cell 130 is used as  
14 the reference memory cell, the current sources 702, 704, 800 can be used to apply the  
15 write currents used to calibrate the memory device 50. If a memory cell 130 in the  
16 memory array 100 is used as the reference memory cell, care should be taken to return the  
17 memory cell 130 to its state before calibration, so that the bit stored in the memory cell  
18 130 is not erased during calibration.

19 The illustrated sense amplifier 600 in Figure 3 is an example of a sensing device  
20 for detecting a binary state of a the memory cells 130 in the memory device 50. In  
21 practice, other sensing devices, such as a trans-impedance sense amplifier, a charge-  
22 injection sense amplifier, a differential sense amplifier, or a digital differential sense  
23 amplifier, for example, can be used. One sense amplifier 600 is illustrated in Figure 3 for  
24 sensing the binary state of the memory cells 130. In practice, a greater number of sensing  
25 devices can be coupled to a memory array. For example, a sense amplifier can be  
26 included for each column conductor in a memory array.

27 The conventions for current flow to write states of 0 and 1 in the memory array  
28 are arbitrary, and can be reassigned to fit any desired application of the memory device  
29 50.

30 The memory cells 130 used in the memory array 100 can be any type of memory  
31 cell responsive to write currents. In one embodiment, the memory cells 130 and the  
32 reference memory cell 160 are magnetic random access memory (MRAM) cells. Other  
33 cells are also appropriate for use in the memory array 100. For example, memory cells

1 such as giant magnetoresistance (GMR) devices, magnetic tunnel junctions (MTJ), and  
2 other types of memory cells may be used in the memory array 100.

3 The memory device 50 can be used in a wide variety of applications. One  
4 application may be a computing device having an MRAM storage module. The MRAM  
5 storage module may include one or more MRAM memory arrays for long term storage.

6 MRAM storage modules can be used in devices such as, for example, laptop  
7 computers, personal computers, and servers.

8 A temperature compensated voltage source in accordance with the above  
9 embodiments could also be used in conjunction with a memory array.

10 While the memory device 50 is described with reference to exemplary  
11 embodiments, many modifications will be readily apparent to those skilled in the art, and  
12 the present disclosure is intended to cover variations thereof.